REH DESIGN

# CPU280

Hardware-Manual

## 1. Overview

The CPU280 is a complete computer using the single-board euro form factor (100 x 160 mm). It was designed to maximally employ the power of the Z280 processor chip with minimal circuit complexity. Functions which are possible but not used in practice were not realised, in favor of a simple and clear design. Due to the complete code compatibility between Z80 and Z280, existing software (for example under cp/m) can continue to be used. Future software can benefit from the higher power and larger instruction set of the Z280.

The board includes two EPROMs for a total of 64 KB or 128 KB of firmware, 512 KB to 4 MB of dynamic memory, a real-time clock with battery backed-up RAM, a floppy controller for up to four drives, and two V.24 (RS-232) serial ports. Connection to other external devices is made via an ECB-bus interface. Additionally, three jumpers can be read and three LEDs driven by software, for example for system configuration information and 'hard' errors.

In the CPU280, the Z280 MPU chip is set up for maximal throughput: 16-bit Z-Bus, clock ratio 1:1 (external bus clock equals internal clock) at clock frequencies up to 12.5 MHz. These clock rates are too fast for the ECB-bus, nor are peripheral chips available; therefore external I/O accesses are slowed down with 4 wait-states, and the bus timing stretched, making the external bus clock only half the CPU clock (6 MHz).

The design of the CPU280 is kept very straightforward, and the timing is generated completely synchronously. That yields high reliability, independence from chip lot variations and temperature, but also easy debugging. The PC board is a simple two-layer board, which avoids unneccessary costs. The CPU280 works on a single 5 V supply, drawing about 350 mA.

## 2. Circuit Description

### 2.1 Reset, CPU and address space

On the CPU280 board, a power supply supervisor (IC5) generates a reliable reset signal, as long (or whenever) the supply voltage drops below 4.6 V. The board can also be reset via the reset-input on the ECB bus. The buffered reset signal is available at the 'reset-out' pin for other boards on the bus. To satisfy the Z280's requirements on the speed of reset transitions, the reset signal for the CPU is buffered through a GAL.

The configuration of some of the Z280's important CPU timing parameters can only happen during reset. For that, the /WAIT signal has to be asserted during the rising edge of /RESET, while the desired configuration of the bus initalisation register is driven on the data bus D0..D7. In the CPU280, the circuit made up of IC32A and T1 does that, while the jumpers J1..J4 and the resistors RN2, RN6 and R4..R7 provide the correct data bits. The jumpers J1..J4 select the number of wait-states for the EPROM and the CPU clock ratio (internal/external). The other adjustable parameters are not useful for the CPU280, and therefore not accessible through jumpers.

The system clock is generated by the CPUs internal crystal oscillator. The choice of clock frequency depends on the grade of CPU chip used, but should be a multiple of 2.4576 MHz, so the CPU-internal serial port can operate at a standard baud-rate. That yields clock frequencies of 9.8304 MHz or 12.288 MHz (using the 10 MHz or 12.5 MHz chip). Should faster versions of the Z280 become available, J1 and J2 can be set for a clock ratio of 1:2, which allows for a CPU clock of up to 25 MHz with the rest of the board still operating at 12.5 MHz.

All MPU signals which are not used on the board (control lines for DMA and timer) are available on solder jumpers, with all CPU inputs preconnected to ground. That leaves no CMOS inputs floating, and the signal can easily be identified and picked up at the solder jumpers, and routed via jumper cables to external peripherals.

With the internal MMU (memory management unit), the Z280 has a total address space of 16 MB, with timing parameters adjustable independantly for the two 8 MB parts of the address space. Since the processor starts executing at address 0 after a reset, the lower half is used for the EPROM. The upper half addresses the on-board dynamic RAM.

The I/O address space of the Z280 is also 16 MB, with the uppermost 8 address bits supplied by the 'I/O page register'. The lower 16 bits are formed from CPU registers, just as in the Z80. Since all I/O instructions only use 8 address bits officially, the middle 8 bits (A8 through A15) are not decoded (that is ignored) for I/O accesses on the CPU280. The I/O page register selects different I/O groups, with 256 addresses available in each page. The Z-bus is 16 bits wide for memory accesses, and 8 bits wide for I/O accesses. Therefore 8-bit peripherals can be used throughout, even though the memory bus on the board is 16 bits wide.

Consult the Z280 data sheet and the 'technical manual' for more information about the Z280 processor itself, in particular about use and programming of the internal peripherals.

### 2.2 EPROM

The on-board EPROM is realized using IC9 and IC10. That yields a maximum capacity of 32K x 16 bits (i.e. 64 kB using 27C256 chips) or 64K x 16 bits (i.e. 128 kB using 27C512 chips). Jumper J5 selects which chip type is being used. Neither a mix of those two chips nor other EPROM types are supported.

The EPROM uses the physical addresses 000000-00FFFFh or 000000-01FFFFh. Since the higher address lines are not decoded, 'mirroring' occurs: the EPROM is visible 128 or 64 times in the lower 8 MB of memory.

Since the EPROM is usually accessed only once while booting (just long enough to copy it into RAM), wait-states can be used for accessing it; that means the speed of the EPROMs is not critical; low-cost 200 or 250 ns chips are completely sufficient. At maximum clock frequency (12.5 MHz) one can use 150 ns EPROMs without wait states, 200 ns with one wait, and 250 ns with two waits. The number of wait states for the EPROMs is selected using jumpers J3 and J4.

### 2.3 DRAM, Burst-Mode

The core memory of the CPU280 consists of the dynamic RAMs IC11 through IC18. Several different configurations are possible, using 1 MB and 4 MB chips, organized as 256K x 4 or 1M x 4 (part numbers 514256 or 514400). For space reasons, and due to the availability of pin-compatibe types, RAM chips in ZIP packages are used.

The smallest configuration contains four 514256 (IC11 through IC14), which yields a capacity of 512 KB. The standard configuration is eight of these memory chips for a capacity of 1 MB. Memory space can be increased to 2 MB and 4 MB by using four or eight 514400 chips. When changing between 256Kx4 and 1Mx4 chips, the programming of IC22 has to be modified.

The RAM uses physical addresses beginning at 800000h, in the largest configuration through BFFFFFh. The RAM chips should have 80 ns access time, to ensure reliable operation at the maximum clock frequency. The RAM is always used without wait states. Selecting additional wait states for RAM accesses (by programming the CPU bus timing and control register) is illegal, due to the timing of the burst mode accesses. The Z280 is able to use a special memory access when loading instructions from external memory into the internal cache (opcode fetch), with faster data transfer. It begins a regular memory access, but then reads the content of four memory words in four consecutive clock cycles, in a burst without additional address information from the CPU. This access mode is about twice as fast as reading individual memory words. In order to use this mechanism,

special RAM types can be used (known as nibble mode RAMs), which can automatically access four addresses for consecutive accesses to a memory row. Since those RAMs are not available in the 4-bit wide organisation (and with 1-bit wide RAMs at least 16 RAM chips would be required), the CPU280 generates the addresses for burst mode accesses outside the RAMs with additional hardware. The RAMs are being used in the standard 'fast page mode', and receive a new address and a CAS pulse for each additional access. That makes it possible to achieve the same throughput using low-cost standard RAM chips, with additional flexibility.

All the timing signals for the dynamic RAMs are generated synchronously, i.e. controlled only by the CPU clock. This results in very reliably operation, even under varying conditions (for example temperature, supply voltage), and eliminates the need for adjustment. Only the length of the CAS pulse in burst mode is generated from a gate delay, and can be optimized by changing C6 (the pulse is too short to be generated synchronously).

## 2.4 ECB-Interface and I/O-Timing

The ECB interface consists mostly of drivers for the data, address and control bus (IC6 through IC8), plus the clock generation in IC4A. This ECB interface supports only I/O accesses, since 16 bit wide memory accesses are simply not possible. An additional interface to adapt memory accesses to the ECB bus is in principle possible, but rather demanding. Furthermore, the maximum memory capacity on board should be sufficient for all uses.

Therefore, only signals required for I/O accesses are routed to the ECB bus. The interrupt inputs of the CPU are connected to the bus without buffers, but with pull-up resistors. Those signals which are never active (/MRQ and /BUSAK) are connected to Vcc via solder jumpers, which are open by default; if the bus is not terminated adequately that can be used to tie these signals to well-defined potentials. For external boards which contain dynamic memories (for example RAM disks) a refresh signal is available; it becomes active every 15.6 µs for the duration of one memory access (240 ns at 12.5 MHz clock frequency), assuming the CPU-internal refresh controller has been programmed in the usual fashion.

External I/O boards on the ECB bus are accessed through their own I/O page, so the full I/O address space of the bus is available. Due to lack of board space and the 8-bit address space of the Z80 family, only the lower 8 address bits (A0 through A7) are connected to the ECB bus, which makes for 256 usable addresses. That should be far more than enough for most applications.

I/O accesses generally require four wait states to generate the correct bus timing. The bus clock is generated by dividing the CPU clock by two using IC4A, which is synchronized to /AS at the beginning of each bus transaction. Therefore the sequence of control signals and clock on the external bus is the same as for a Z80 CPU running at 6 MHz. The synchronization is necessary for some Z80 peripherals (for example the Z80-PIO), which won't function correctly without it.

Interrups from ECB boards are fully supported by the CPU280. The /INT line from the bus is connected to the INTA input of the CPU, and can be vectorized by the CPU. The interrupt sources on the CPU280 use other INT inputs, so the interrupt from the ECB bus can be used independently of the internal interrups. Due to wait states the interrupt-acknowledge transaction also emulates a 6 MHz Z80 CPU. Since the RETI transaction works in memory (and therefore too fast for the external bus), and since the Z280 CPU uses a special RETI instruction in interrupt mode 3, and since no M1 signal is available, a slow artifical Z80 RETI transaction has to be generated for the external bus. It consists of two consecutive accesses, each with /M1 and /RD but without /IORQ being active, and with the bytes EDh and 4Dh on the data bus. These signals are generated on the CPU280 by accessing a special I/O page, which activates the /M1 line on the external bus. Reading two memory cells of the real-time clock's NVRAM (which have to be initialized to the correct information) generates the correct slow signals on the bus. This allows true bus compatibility to a 6 MHz Z80 even when using interrupts.

## 2.5 Real-time clock and NV-RAM

The DS 1287 (A) chip (IC27) is used for the real-time clock. It contains the actual real-time clock with alarm and calendar, a programmable square wave and interrupt source, plus 50 bytes of non-volatile memory (NVRAM). The lithium battery necessary for battery backup of the clock and NVRAM is contained in the same package; therefore no external power is necessary, and the setting of clock and NVRAM are not lost if the board is powered down or removed from the bus.

The A-version of the chip can be internally reset by setting jumper j10 (only while the power is off). The interrupt output is connected to interrupt B of the CPU, together with the serial port IC31, and uses a fixed vector in the CPU. The square wave output of the real-time clock is connected to one bit of the GPI (see section 2.8), and can be read from there.

For further details on registers of the real-time clock and its programming, see the data sheet for the DS 1287.

## 2.6 Floppy controller

The floppy controller uses the FDC 37 C 65 B/C chip (IC28, also known as GM 82 C 765), which forms the interface between the CPU and the drives without additional hardware. It contains the actual FDC (a 765 core), two clock oscillators, a PLL for reading data, and the high-current 48 mA drivers for the FDD interface. Up to four drives can be connected, with individually settable drive size and format. All floppy-disk formats following the IBM 3740 standard can be used. It is even possible to use 5.25" HD-drives without rotational speed control for normal DD floppies, using the second crystal oscillator at 9.6 MHz. The floppy controller is serviced by DMA channel 0 from the CPU, which allows floppy accesses from a background process. The INTC line of the CPU is used exclusively by the FDC. The pinout of the connector for floppy disk drives (CN2) matches the standard for 3.5" and 5.25" drives; for 8" drives some lines have to be rerouted in the cable.

Since usually rather short cables are used, the FDD-signals are terminated with 330 Ohm instead of the more usual 150 Ohm, which uses less current for 'heating'. If longer cables are to be used, RN3 can be replaced by a lower resistance network.

When using 5.25" HD drives with DD floppies, a transistor (T2) switches pin 2 of the drive interface (low density) to low, controlled by the 'DRV' signal from the GPO. This signal is not required for 3.5" drives; they sense the density using the additional hole for HD floppies.

## 2.7 Serial interfaces

The CPU280 contains two V.24 (RS-232) serial line interfaces. One is the CPU-internal UART, while the second is implemented using the 'Twenty-pin UART' chip (COM 81 C 17, IC31). The latter supplies all the signal required for modem control (two data and two handshake lines), whereas the CPU-internal UART only supports data lines. The handshake lines for the CPU-internal interface are generated from single-bit I/O lines, using the GPIO (see section 2.8).

Both interfaces can generate interrupts. The CPU-internal interface has its own interrupt level in the CPU chip, whereas the TPUART shares the INTB line with the real-time clock.

Both interfaces support baud rates of 50 through 38400 baud (assuming a commensurate clock frequency for the CPU), using

7 or 8 data bits, 1 or 2 stop bits, and optional even or odd parity.

The level conversion is done using the driver chip IC29 (LT 1134), which contains four V.24 receivers and transmitters and the DC-DC converter for 5V operation.

### 2.8 General-Purpose-I/O (GPIO)

Several single-bit I/O requirements use IC25 and IC26. Bit output is done with an addressable 8-bit latch (IC25). Both its address and data inputs are connected to the address bus; that allows setting and resetting bits by accessing various addresses, regardless of the data bus. During reset all outputs are set to 0.

Four of the eight outputs are used for various control functions (handshake for CPU-UART, motor-on for the floppy disk drives, control signals for the FDC), another three outputs drive LEDs, which can for example be used to signal hard errors. One output is connected to one of the GPIO input lines. This can be used after a CPU reset to check whether the reset was generated by hardware from the /RESET line, or by software by jumping into the cold-start routine.

For bit input a simple bus driver (IC26) is used. In addition to the reset flag, it reads the CTS-signal from the CPU-UART serial interface, the square wave signal from the real-time clock, and three user-selectable jumpers (J7 through J9).

## 3. Assembly, Debugging

The PC board of the CPU280 is assembled in the usual order: First the flatter components, then proceedings in order of increasing height. When installing the crystals always use an isolating spacer between them and the board! One can use special plastic or mica washers, or in emergencies just electrical tape. Since the special sockets for the ZIP-RAMs may be hard to find, one can use SIL socket strips. With the RAMs in sockets, the board closely fits into a standard-width slot in an euro-crate (4 TE, or .800" = 20.32mm).

The floppy connector CN2 can be mounted on the component side (use the pads closer to the center or the board) or on the solder side (closer to the edge of the board). This allows routing the floppy drive cable on either side of the board (depending on where you mount the CPU280 board).

For the initial checkout, a test program in EPROMs might be inserted into the CPU280 which tests every hardware component and outputs diagnostic information through one of the serial ports or the LEDs on the board. As it is now, the boot loader program for cp/m+ performs some hardware tests, so one can also get the board running with that program. A completely stuffed CPU280 should draw no more than 400 mA of supply current (for safety reasons best checked initially on a current-limited supply).

As mentioned before, it is recommended to measure the length of the CAS pulse in burst mode. This time is determined by the gate delay of the GALs and by the RC delay of R8 and C6; it should be about 20 ns. If necessary, C6 can be changed to adjust this pulse length.

## 4. Jumpers and solder jumpers

The CPU280 contains a total of 10 settable jumpers, used to adjust various system configuration parameters. In addition, there are 12 solder jumpers, which allow connecting a few signals to fixed potentials. Both types are listed here.

**J1,J2** These two jumpers determine the clock scaling (ratio of external clock). The possible combinations are:

| | | |
|---|---|---|
| J1 connected | J2 connected | Ratio 2:1 |
| J1 open | J2 connected | Ratio 1:1 (default) |
| J1 connected | J2 open | Ratio 4:1 |
| J1 open | J2 open | Illegal |

**J3,J4** These two jumpers determine the number of wait states for EPROM access as follows:

| | | |
|---|---|---|
| J3 connected | J4 connected | 0 Wait-states |
| J3 open | J4 connected | 1 Wait-state |
| J3 connected | J4 open | 2 Wait-states |
| J3 open | J4 open | 3 Wait-states |

**J5** Selects the EPROM type:
J5 towards the CPU: 27 C 256 (preconnected!) J5 towards the RAM: 27 C 512

**J6** Precompensation of the FDC on the innermost tracks:
J6 connected: 187 ns
J6 open: 125 ns (default)

**J7-J9** User configuration jumpers, read in by the GPI

**J10** Internal reset of the RTC (use only when power off)

| | |
|---|---|
| LJ1 | Connects ECB signals /MRQ with VCC |
| LJ2 | Connects ECB signals /BUSAK with VCC |
| LJ3-5 | Connects CPU-Pin CTIO0-2 with GND |
| LJ6-8 | Connects CPU-Pin CTIN0-2 with GND (preconn.) |
| LJ9-10 | Connects CPU-Pin /DMASTB0-1 with GND |
| LJ11-12 | Connects CPU-Pin /RDY1-2 with GND (preconn.) |

## Appendices

### A1. Parts list

| | |
|---|---|
| IC1 | Z 280 MPU, 12.5 MHz (or 10 MHz) |
| IC2-3 | 74 HCT 373 |
| IC4 | 74 HCT 74 |
| IC5 | TL 7705 |
| IC6,IC8 | 74 ACT 244 (or ALS) |
| IC7 | 74 ACT 245 (or ALS) |
| IC9-10 | 27 C 256 or 27 C 512 |
| IC11-18 | 514256-80 or 514400-80 (ZIP) |
| IC19-20 | 74 ACT 158 (or AS) |
| IC21-24 | GAL 16V8 Q-25 |
| IC25 | 74 HCT 259 |
| IC26 | 74 HCT 367 |
| IC27 | DS 1287 (or MK 48T87, BQ 3287) |
| IC28 | FDC 37C65 B/C (PLCC) or GM 82C765 |
| IC29 | LT 1134 |
| IC30 | 74 ACT 175 (or AS) |
| IC31 | COM 81C17 |
| IC32 | 74 HCT 14 |
| T1,T2 | BC 547 B or any small-signal NPN transistor |
| D1-D3 | LED 3 mm red |
| | |
| Q1 | 24.576 MHz HC-18U (or 19.6608 MHz) |
| Q2 | 16.000 MHz HC-18U |
| Q3 | 9.600 MHz HC-18U |
| Q4 | 5.0688 MHz HC-18U |
| | |
| C1,C2 | 10p ceramic .200" (18p if Q1=19.6608 MHz) |
| C3 | 10µ Tantalum .100" |
| C4 | 100n ceramic .200" |
| C5 | 1n ceramic .200" |
| C6 | 120p ceramic .200" (best measured and fitted) |
| C7 | 15p ceramic .200" |
| C8 | 47p ceramic .200" |
| C9 | 56p ceramic .200" |
| C10 | 68p ceramic .200" |
| C11-C14 | 1µ Tantalum .100" |
| CK1-CK27 | 25x 100n ceramic .200", 2x 10µ Tantalum .100" |
| | |
| R1,R2 | 4 k 7 |
| R3,R9,R10 | 1 k |
| R4-R7 | 3 k 3 |

| | | |
|---|---|---|
| R8 | | 100 R |
| R11 | | 10 k |
| RN1 | | RSIL 5x 2 k 2 |
| RN2,RN6 | | RSIL 4x 3 k 3 |
| RN3 | | RSIL 5x 330 R |
| RN4 | | RSIL 5x 4 k 7 |
| RN5 | | RSIL 3x 330 R (solder from three resistors) |
| CN1 | ECB | VME-type connector, 64 pins, rows a and c Type DIN 41612 C |
| CN2 | FDD | Header 50-pin (2x25), on component or solder side |
| CN3 | V.24 | Header 20-pin (2x10) |
| J1-J4 | | Header 2x4, CPU-Init |
| J5 | | Header 1x3, EPROM-Typ |
| J6-J9 | | Header 2x4, FDC-Precomp and User-Jumpers |
| J10 | | Header 1x2, RTC-Reset |

## A2. Connector pinouts:

**Pinout CN1 (ECB-BUS):**

| a | Nr | c |
|---|---|---|
| +5V | 1 | +5V |
| D5 | 2 | D0 |
| D6 | 3 | D7 |
| D3 | 4 | D2 |
| D4 | 5 | A0 |
| A2 | 6 | A3 |
| A4 | 7 | A1 |
| A5 | 8 | |
| A6 | 9 | A7 |
| /WAIT | 10 | |
| | 11 | IEI |
| | 12 | |
| | 13 | |
| | 14 | D1 |
| | 15 | |
| 2xCLK | 16 | IEO |
| | 17 | |
| | 18 | |
| | 19 | |
| /M1 | 20 | /NMI |
| | 21 | /INT |
| | 22 | /WR |
| | 23 | |
| | 24 | /RD |
| | 25 | |
| | 26 | /RESOUT |
| /IORQ | 27 | |
| /RFSH | 28 | |
| | 29 | CLK |
| | 30 | (/MRQ) |
| (/BUSAK) | 31 | /RESIN |
| GND | 32 | GND |

**Pinout CN2 (Floppy drives):**

| 8" | 5.25" | Signal | Change for 8" drives |
|---|---|---|---|
| 2 | | RWC/RPM | |
| 4 | | MOTOFF | |
| 6 | | MOTOFF | |
| 8 | | MOTOFF | |
| 10 | | nc | |
| 12 | | DCHG | |
| 14 | | SIDE SEL | |
| 16 | | HDLD | |
| 18 | 2 | RWC/RPM | HDLD (16,20) |
| 20 | 4 | HDLD | INDEX (24) |
| 22 | 6 | DS3 | nc |
| 24 | 8 | INDEX | MOTOFF (4,6,8) |
| 26 | 10 | DS0 | |
| 28 | 12 | DS1 | |
| 30 | 14 | DS2 | |
| 32 | 16 | MOTON | DS3 (22) |
| 34 | 18 | DIRECTION | |
| 36 | 20 | STEP | |
| 38 | 22 | WRITE DATA | |
| 40 | 24 | WRGATE | |
| 42 | 26 | TRK0 | |
| 44 | 28 | WRPROT | |
| 46 | 30 | READ DATA | |
| 48 | 32 | SIDE SEL | (nc) |
| 50 | 34 | DCHG | (nc) |

(1..49 odd pins: GND)

**Pinout CN3 (V.24 ports):**

The pinout allows directly connecting two 9-pin DSUB connectors on the flat cable coming from this connector, and their pinout will match a serial port on a DSUB-25 connector:

| CN3 | DSUB | Signal | |
|---|---|---|---|
| 1 | 1 | GND | Ground (frame ground 1) |
| 2 | 6 | nc | |
| 3 | 2 | TXD 1 | Transmit data 1 |
| 4 | 7 | GND | Ground (signal ground 1) |
| 5 | 3 | RXD 1 | Receive data 1 |
| 6 | 8 | nc | |
| 7 | 4 | RTS 1 | Request-to-Send 1 |
| 8 | 9 | nc | |
| 9 | 5 | CTS 1 | Clear-to-Send 1 |
| 10 | - | nc | |
| 11 | 1 | GND | Ground (frame ground 2) |
| 12 | 6 | nc | |
| 13 | 2 | TXD 2 | Transmit data 2 |
| 14 | 7 | GND | Ground (signal ground 2) |
| 15 | 3 | RXD 2 | Receive data 2 |
| 16 | 8 | nc | |
| 17 | 4 | RTS 2 | Request-to-Send 2 |
| 18 | 9 | nc | |
| 19 | 5 | CTS 2 | Clear-to-Send 2 |
| 20 | - | nc | |

## A3. GAL Programs

```
TITLE       CPU280 RAM-TIMING AND NIBBLEMODE IC21
AUTHOR      TILMANN REH
COMPANY     REHDESIGN
DATE        23.07.1990

CHIP Z280RAM 16V8

NCLK A3 A1 A2 A4 IE DS OE MQD GND
QOE MUX WR MA0 MA1 RES CPURES MQA FFR VCC

EQUATIONS

/WR     = /OE * /DS
MA0     := /MQA * A3 + MQA * /MUX * A1 + MUX * /MA0
MA1     := /MQA * A4 + MQA * /MUX * A2
         + MUX * MA0 + MUX * MA1
/FFR    = IE * DS * MQD
CPURES  = RES
```

```
TITLE       CPU280 CAS-DECODER IC22
AUTHOR      TILMANN REH
COMPANY     REHDESIGN
DATE        31.10.1990

CHIP Z280CAS 16V8

CLK RW BW RFSH A0 A19 A20 A21 A22 GND
MUX BRF NCK CAS1L NCLK CAS0H CAS0L MQA CAS1H VCC

EQUATIONS
```

```
BRF    = /RFSH
NCLK   = /CLK

/CAS0L = MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * BW * A0
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * CLK
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * NCK
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * /RW
       + RFSH * /MUX * MQA

/CAS0H = MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * BW * /A0
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * CLK
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * NCK
       + MUX * /RFSH * /A22 * /A21 * /A20 * /A19 * /BW * /RW
       + RFSH * /MUX * MQA

/CAS1L = MUX * /RFSH * /A22 * /A21 * /A20 * A19 * BW * A0
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * CLK
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * NCK
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * /RW
       + RFSH * /MUX * MQA

/CAS1H = MUX * /RFSH * /A22 * /A21 * /A20 * A19 * BW * /A0
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * CLK
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * NCK
       + MUX * /RFSH * /A22 * /A21 * /A20 * A19 * /BW * /RW
       + RFSH * /MUX * MQA


TITLE      CPU280 SYSTEM-SIGNALS IC23
AUTHOR     TILMANN REH
COMPANY    REHDESIGN
DATE       02.12.1990

CHIP Z280SYS 16V8

ST3 ST2 ST1 ST0 AS DS A21 A22 A23 GND
MQA MDA NAS ROM BIO M1 RFSH NNAS XIO VCC

EQUATIONS

NAS    = /AS
NNAS   = NAS
/ROM   = ST3 * /A23 * /DS
MDA    = ST3 * A23 * /A22 * ( /AS + NAS + NNAS )
       + /ST3 * /ST2 * /ST1 * ST0 * ( /AS + NAS + NNAS )
       + MQA
RFSH   = /ST3 * /ST2 * /ST1 * ST0
/BIO   = /ST3 * /ST2 * ST1 * /ST0 * /A23 * /A22 * /A21 * /DS
       + /ST3 * ST2 * /ST1 * /ST0
/XIO   = /ST3 * /ST2 * ST1 * /ST0 * /A23 * /A22 * A21
       + /ST3 * /ST2 * ST1 * /ST0 * /A23 * A22 * /A21
/M1    = /ST3 * ST2 * /ST1 * /ST0
       + /ST3 * /ST2 * ST1 * /ST0 * /A23 * /A22 * A21


TITLE      CPU280 IO-ADRESS-DECODER IC24
AUTHOR     TILMANN REH
COMPANY    REHDESIGN
DATE       16.12.1990

CHIP Z280IO 16V8

NC NC XIO DS A6 A5 A7 OE IE GND
NC UART GPO GPI RTC DACK LDOR LDRSR FDC VCC

EQUATIONS

/RTC   = /XIO * /A7 * /A6
/FDC   = /XIO * /A7 * A6 * /A5
/DACK  = /XIO * /A7 * A6 * A5 * /DS
/LDOR  = /XIO * A7 * /A6 * /A5
/LDRSR = /XIO * A7 * /A6 * A5
/UART  = /XIO * A7 * A6 * /A5
/GPI   = /XIO * A7 * A6 * A5 * /IE * /DS
/GPO   = /XIO * A7 * A6 * A5 * /OE * /DS
```

## A4. Address space organization memory/IO

| | | |
|---|---|---|
| Memory: | 000000-01FFFF | Boot/System-EPROM |
| | 800000-BFFFFF | max. 4 MB DRAM Onboard |
| I/O: | 00xx00-00xxFF | ECB-Bus (256 addresses) |
| | 20xx00-20xxFF | Onboard-I/O, /M1 on ECB-Bus |
| | 40xx00-40xxFF | Onboard-I/O |
| | FExx00-FFxxFF | Onchip-I/O Z280 |

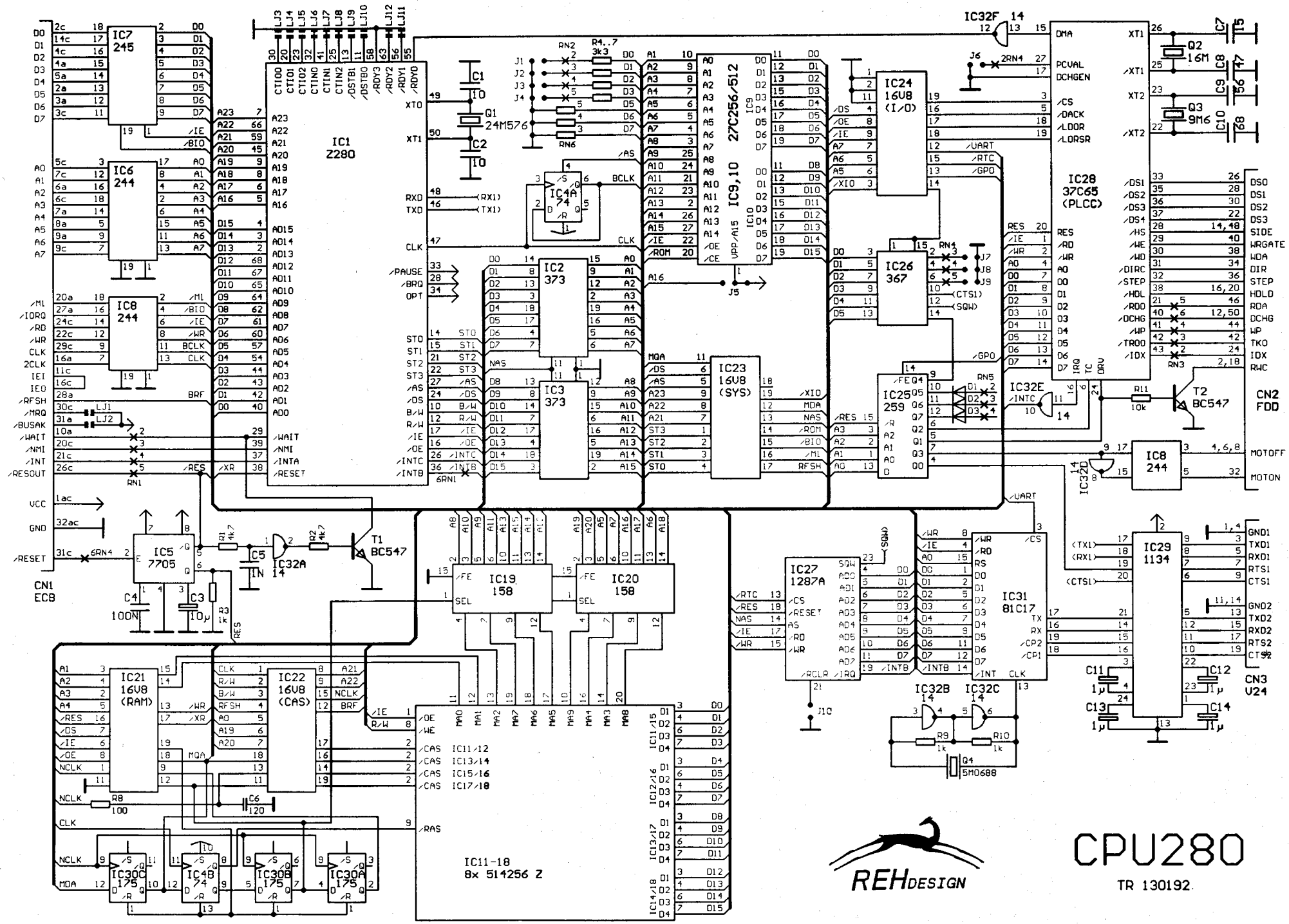
| | | |
|---|---|---|
| Onboard-I/O: | 00-3F | RTC / NVRAM |
| | 40,41 | FDC |
| | 60 | FDC-DACK |
| | 80 | FDC-LDOR |
| | A0 | FDC-LDRSR |
| | C0 | UART |
| | E0-EF | GP-I/O |

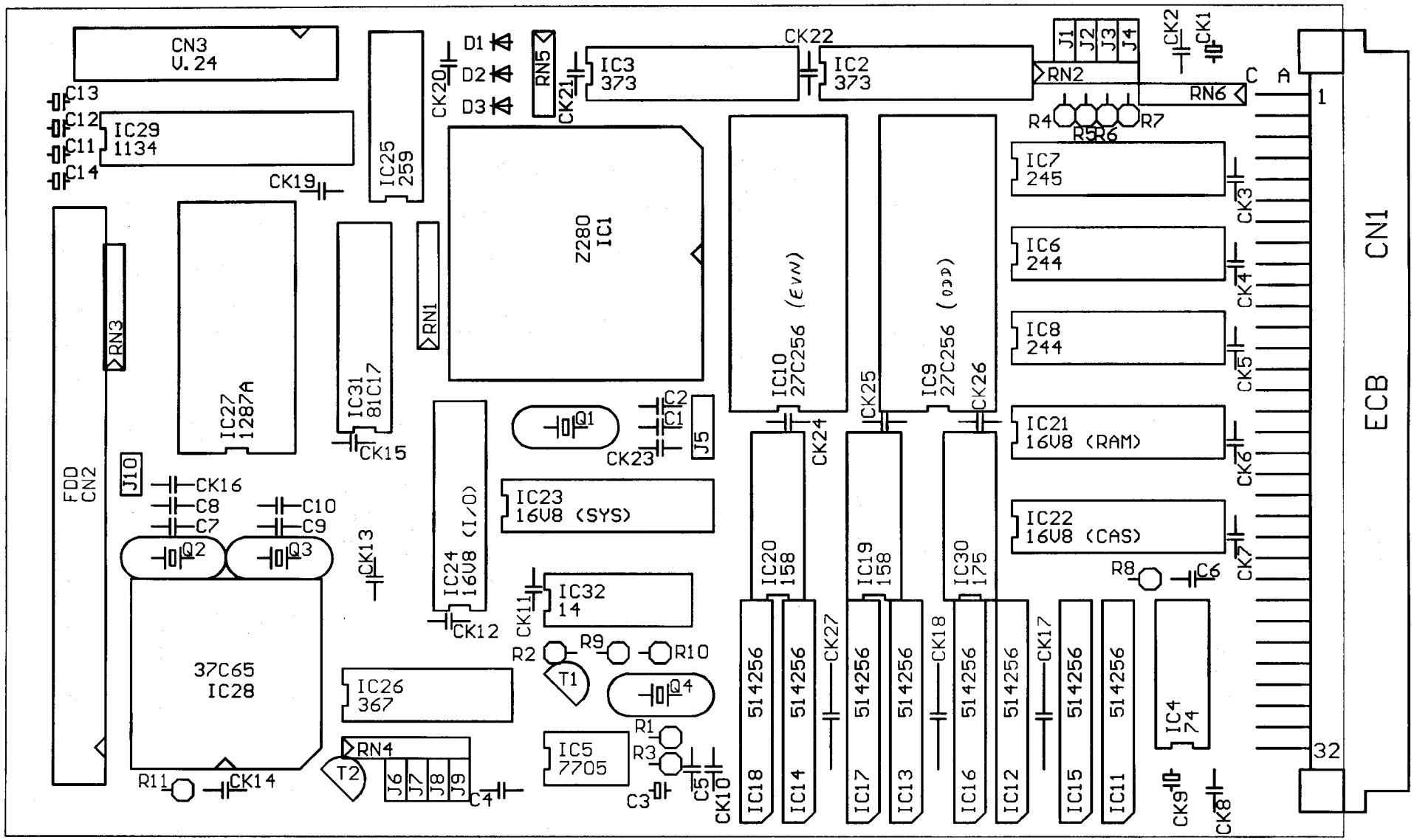
| | | | |
|---|---|---|---|
| GP-Output: | E0 / E1 | RTS1 | off / on |
| | E2 / E3 | DRV | off / on |
| | E4 / E5 | TC | off / on |
| | E6 / E7 | MOTOR | off / on |
| | E8 / E9 | WARM | off / on |
| | EA / EB | LED1 | on / off |
| | EC / ED | LED2 | on / off |
| | EE / EF | LED3 | on / off |

| | | |
|---|---|---|
| GP-Input: | Bit 0 | User-Jumper 1 (J7) |
| | Bit 1 | User-Jumper 2 (J8) |
| | Bit 2 | User-Jumper 3 (J9) |
| | Bit 3 | CTS1 |
| | Bit 4 | SQW |
| | Bit 5 | WARM |

| | | |
|---|---|---|
| Interrupts: | NMI | from ECB-Bus (internal vector) |
| | INTA | from ECB-Bus (int. or ext. vector) |
| | INTB | RTC, TPUART (internal) |
| | INTC | FDC (internal) |

This manual was translated by Ralph Becker.


IC1 Z280
IC2 373
IC3 373
IC4A 74
IC5 7705
IC6 244
IC7 245
IC8 244
IC9,10 27C256/512
IC11-18 8x 514256 Z
IC19 158
IC20 158
IC21 16V8 (RAM)
IC22 16V8 (CAS)
IC23 16V8 (SYS)
IC24 16V8 (I/O)
IC25 259
IC26 367
IC27 1287A
IC28 37C65 (PLCC)
IC29 1134
IC30A 175
IC30B 175
IC30C 175
IC31 81C17
IC32A 14
IC32B 14
IC32C 14
IC32D 14
IC32E 14
IC48 74
Q1 24M576
Q2 16M
Q3 9M6
Q4 5M0688
T1 BC547
T2 BC547
CN1 ECB
CN2 FDD
CN3 V24
REHDESIGN
CPU280
TR 130192.

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